FPGA ADC & TDC for Mu2e experiment

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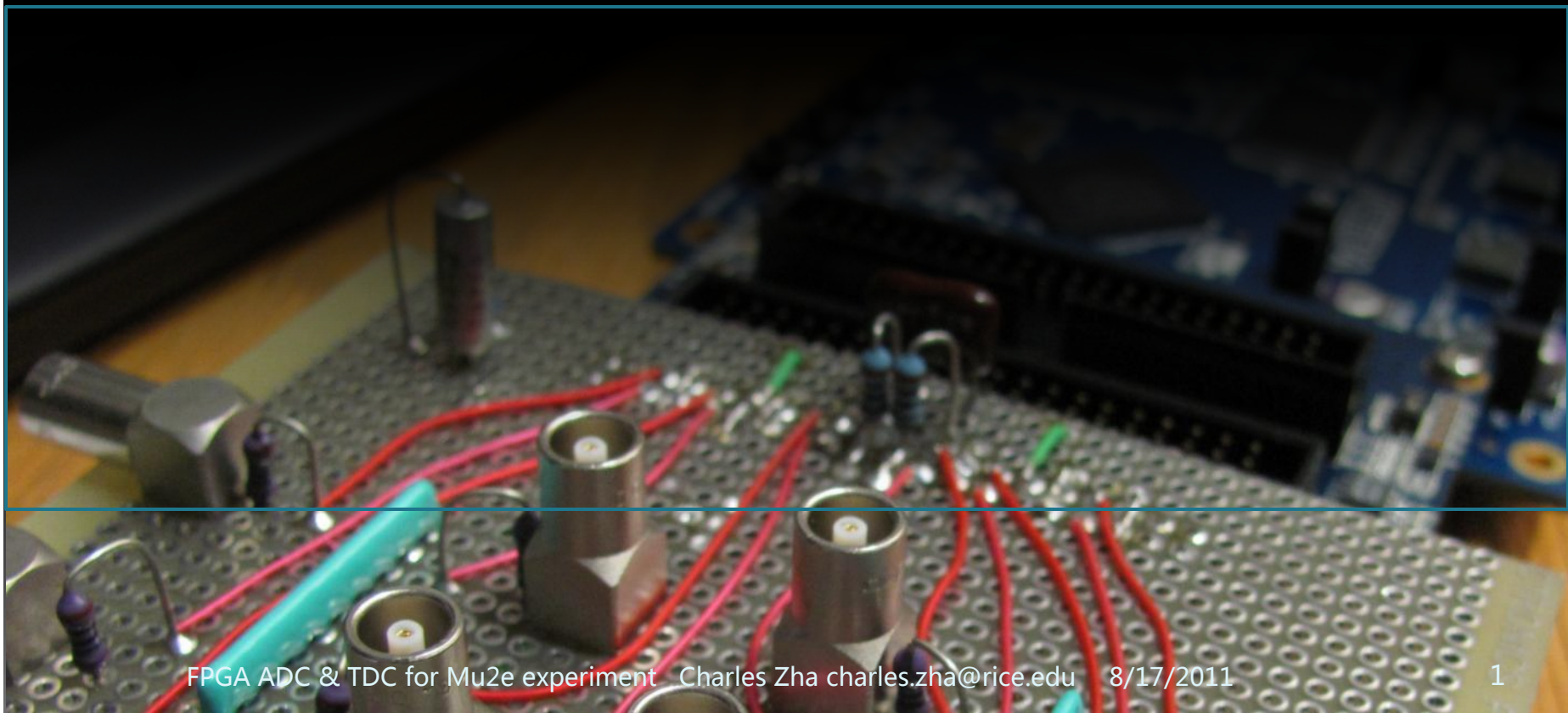
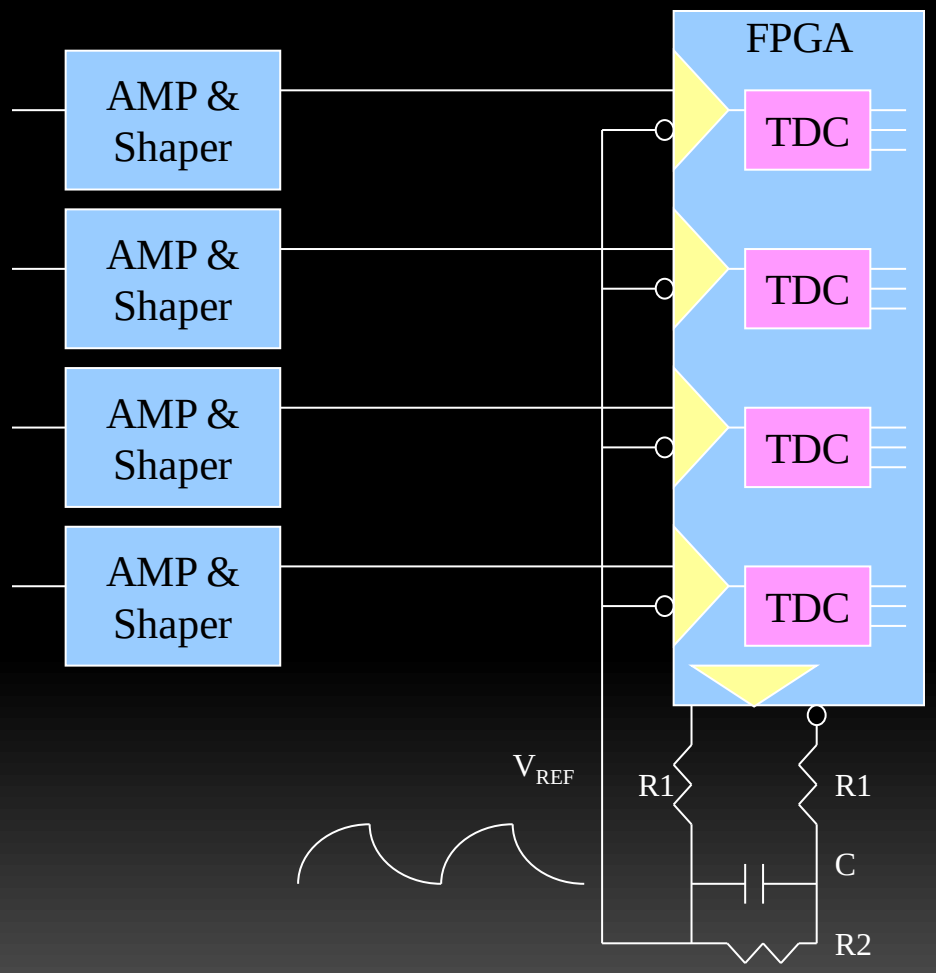


Introduction

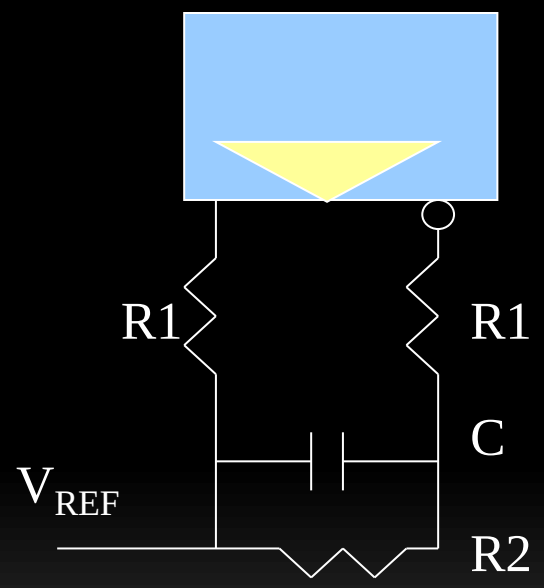
- Digital vs. Analog
  - FPGA = digital
  - ADC = analog
- ADC & TDC implemented entirely in FPGA

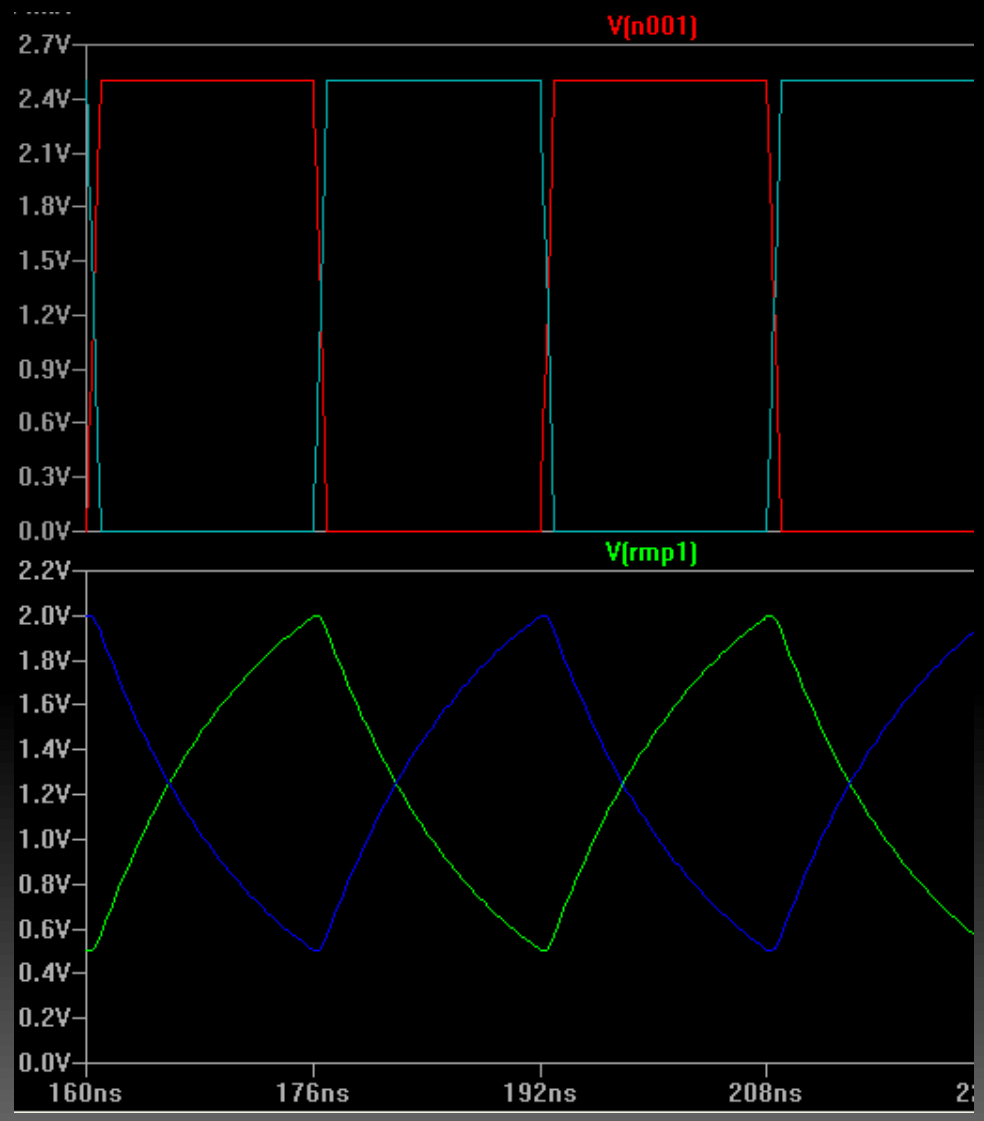
Overview



- Single-slope
- Ramping-comparing scheme

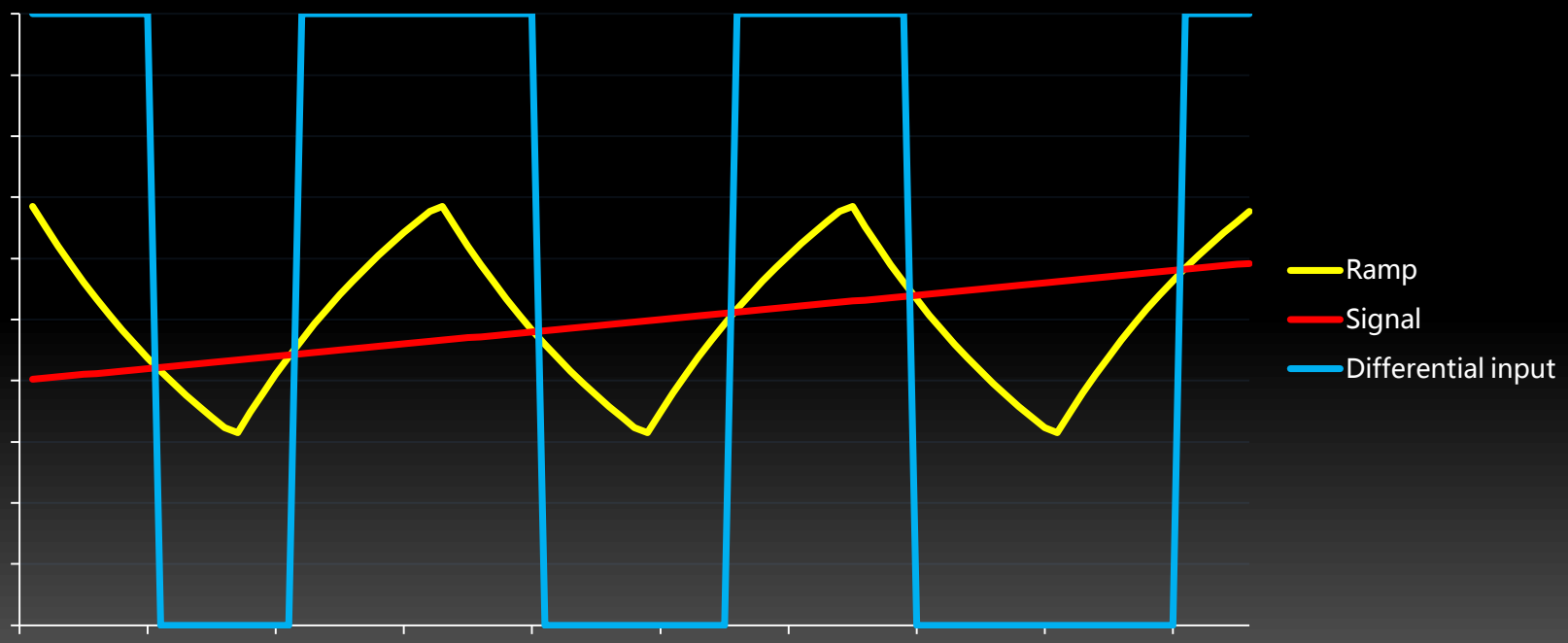
Ramp Generator



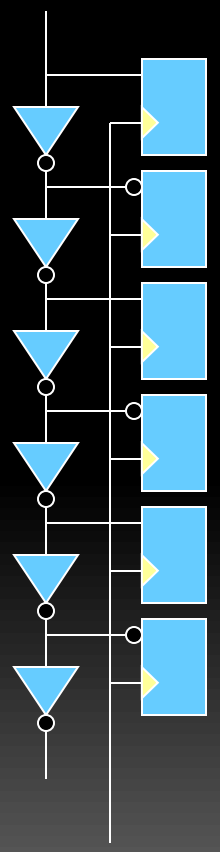


Differential Input

- LVDS input buffers built into FPGA



TDC – Delay Line

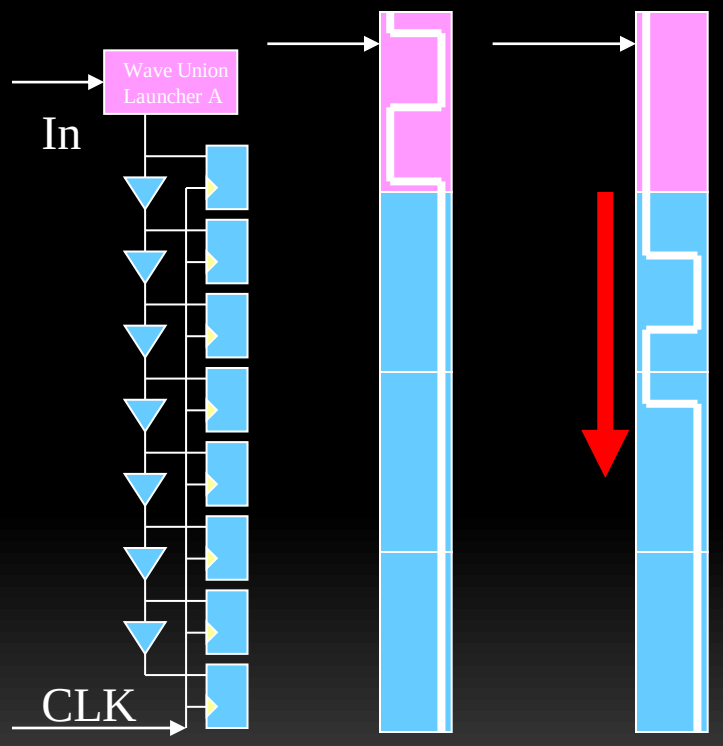


- Register array captures transition edge
- Propagation delay varies:
  - Supply voltage
  - Temperature
  - Logic array block (LAB) structure

TDC – Calibration

- Calibration timing signals sweep entire range
- Histogram booking
- Lookup table translates bin number into time
- Periodic "ultra-wide bins" at LAB boundary

TDC - "Wave Union"



- "Wave Union Launcher" releases 2 0-1 transitions into delay line
- Eliminates ultra-wide bins
- Standard Deviation of 25~30 ps

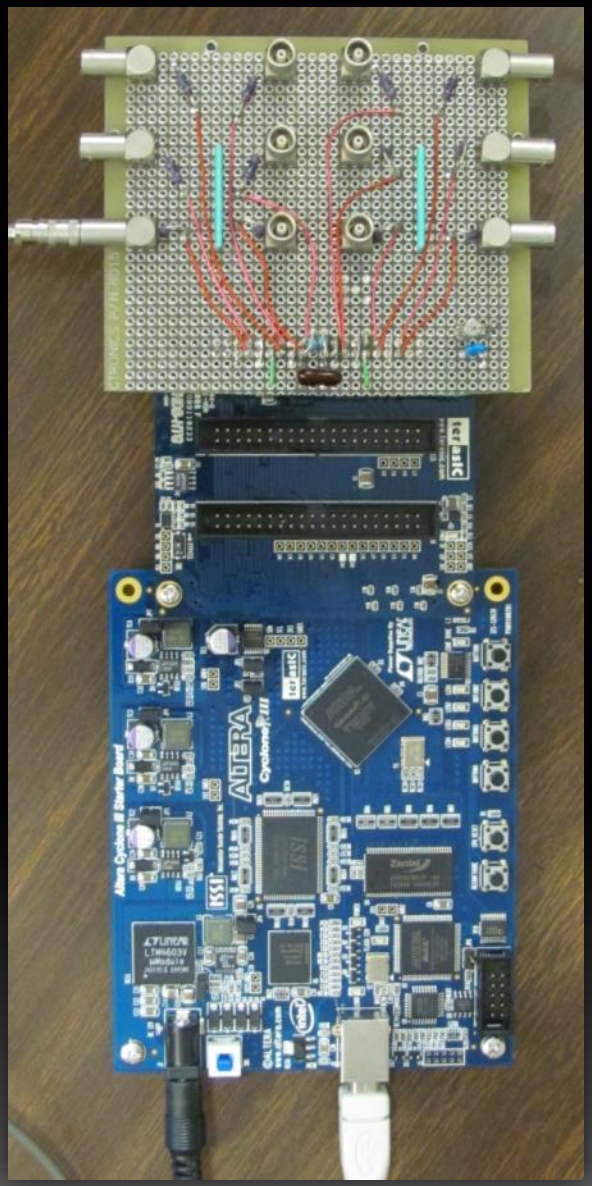
ADC

- Data from TDC contains both time and voltage
- Calculated from exponential response of RC circuit

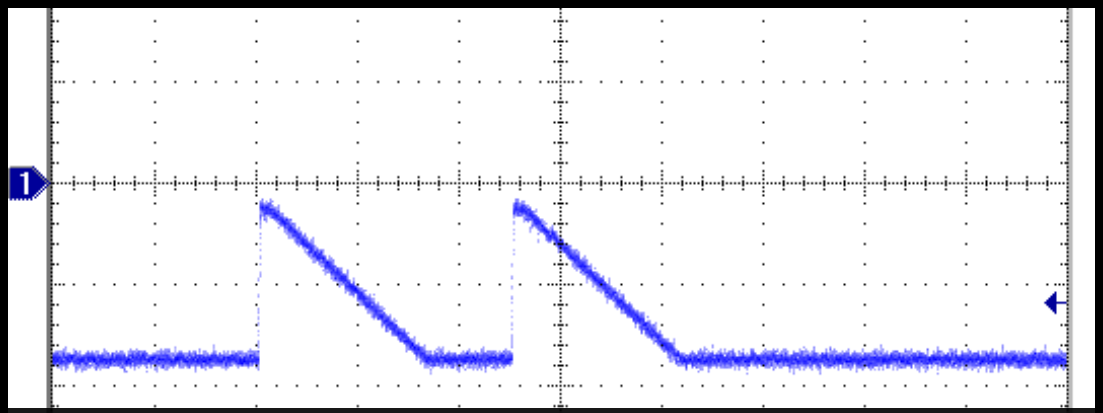
  or
- Calibrated using external DC levels

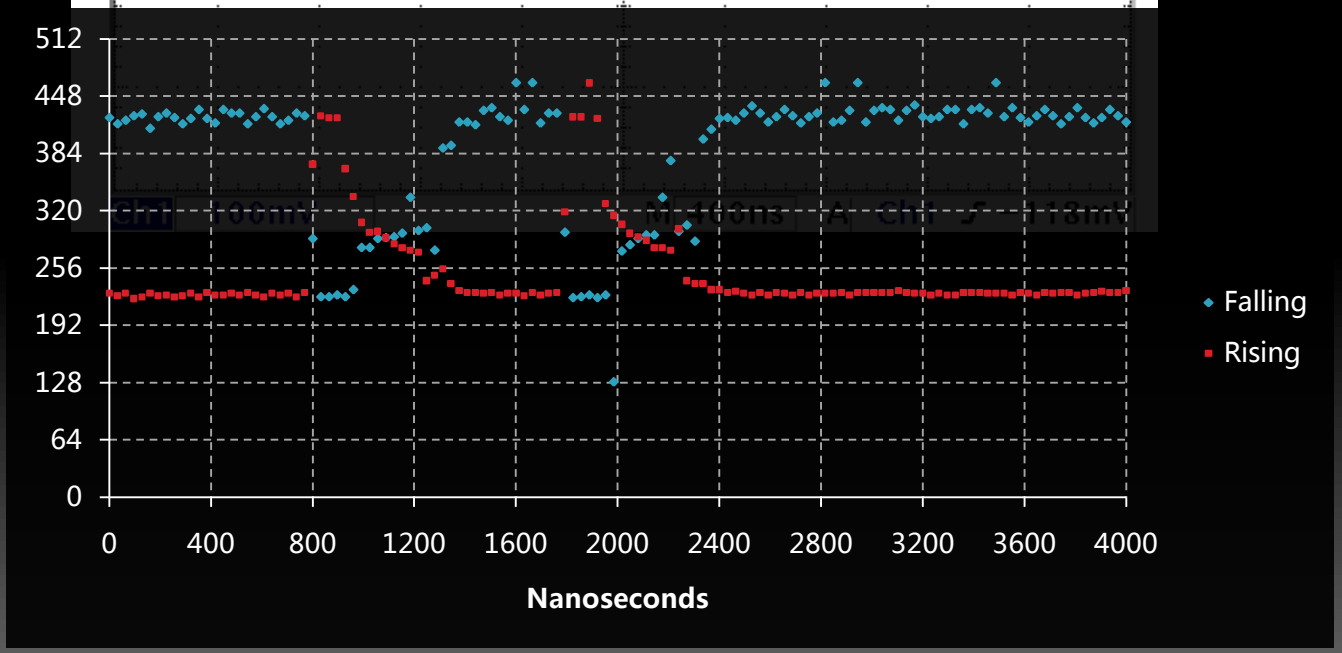
Test platform

- Altera Cyclone III Starter Board
- RC ramping circuit & Input expansion board
  - 12 channels



Test results





Thank You